

CLAIMS

What is claimed is:

- 1 1. A method, comprising:
 - 2 decoding a first instruction into a second instruction and a move
 - 3 instruction;
 - 4 renaming both a first destination register of said second
 - 5 instruction and a second destination register of said move instruction to
 - 6 a physical register; and
 - 7 retiring either said second instruction or said move instruction
 - 8 responsive to a predicate value.

- 1 2. The method of claim 1, wherein said move instruction is
2 responsive to a complement of said predicate value.

- 1 3. The method of claim 1, wherein said decoding includes
2 sending a hint to a register renaming circuit.

- 1 4. The method of claim 3, wherein said sending includes
2 sending said hint via a trace cache.

- 1 5. The method of claim 1, further comprising sequencing said
2 second instruction and said move instruction for out-of-order execution.

- 1 6. The method of claim 5, further comprising, when said
2 second instruction executes before said move instruction and said
3 predicate value is true, squashing said move instruction.

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1 7. The method of claim 6, wherein said squashing occurs
2 before said move instruction executes.

1 8. The method of claim 5, further comprising, when said move
2 instruction executes before said second instruction and said predicate
3 value is false, squashing said second instruction.

1 9. The method of claim 8, wherein said squashing occurs
2 before said second instruction executes.

1 10. A processor, comprising:
2 a decode circuit to decode a first instruction into a second
3 instruction and a move instruction;
4 a register renaming circuit to map a first destination register of
5 said second instruction to a physical register, and to map a second
6 destination register of said move instruction to said physical register;
7 and
8 a retirement circuit to update said physical register with a result
9 of either said second instruction or said move instruction responsive to
10 a predicate value.

1 11. The processor of claim 10, wherein said move instruction is
2 responsive to a complement of said predicate value.

1 12. The processor of claim 10, wherein said decode circuit
2 sends a hint to said register renaming circuit to permit said map of said
3 first destination register and said second destination register to said
4 physical register.

1 13. The processor of claim 12, wherein said hint is sent via a
2 trace cache.

1 14. The processor of claim 10, further comprising a sequencer
2 to permit out-of-order execution of said second instruction and said
3 move instruction.

1 15. The processor of claim 14, wherein said retirement circuit
2 may squash said move instruction when said second instruction
3 executes before said move instruction and said predicate value is true.

1 16. The processor of claim 14, wherein said retirement circuit
2 may squash said second instruction when said move instruction
3 executes before said second instruction and said predicate value is
4 false.

1 17. The processor of claim 14, further comprising execution
2 units to execute said second instruction and said move instruction in
3 parallel.

1 18. A processor, comprising:
2 means for decoding a first instruction into a second instruction
3 and a move instruction;
4 means for renaming both a first destination register of said
5 second instruction and a second destination register of said move
6 instruction to a physical register; and
7 means for retiring either said second instruction or said move
8 instruction responsive to a predicate value.

1 19. The processor of claim 18, wherein said move instruction is
2 responsive to a complement of said predicate value.

1 20. The processor of claim 18, wherein said means for decoding
2 includes means for sending a hint to a register renaming circuit.

1 21. The processor of claim 18, further comprising means for
2 sequencing said second instruction and said move instruction for out-
3 of-order execution.

1 22. The processor of claim 21, further comprising means for
2 squashing said move instruction when said second instruction executes
3 before said move instruction and said predicate value is true.

1 23. The processor of claim 21, further comprising means for
2 squashing said second instruction when said move instruction executes
3 before said second instruction and said predicate value is false.

1 24. A system, comprising:
2 a processor, including a decode circuit to decode a first
3 instruction into a second instruction and a move instruction, a register
4 renaming circuit to map a first destination register of said second
5 instruction to a physical register, and to map a second destination
6 register of said move instruction to said physical register, and a
7 retirement circuit to update said physical register with a result of either
8 said second instruction or said move instruction responsive to a
9 predicate value;
10 a bus to couple said processor to input/output devices; and
11 a communications device coupled to said bus.

1 25. The system of claim 24, wherein said move instruction is
2 responsive to a complement of said predicate value.

1 26. The system of claim 24, wherein said decode circuit sends a
2 hint to said register renaming circuit to permit said map of said first
3 destination register and said second destination register to said
4 physical register.

1 27. The system of claim 24, further comprising a sequencer to
2 permit out-of-order execution of said second instruction and said move
3 instruction.

1 28. The system of claim 27, wherein said retirement circuit may
2 squash said move instruction when said second instruction executes
3 before said move instruction and said predicate value is true.

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- 1 29. The system of claim 27, wherein said retirement circuit may
- 2 squash said second instruction when said move instruction executes
- 3 before said second instruction and said predicate value is false.